WHAT IS CLAIMED IS:

1. A method of forming a capacitor, the method comprising:

providing a workpiece, the workpiece including at least one capacitor region and at least one transistor region;

depositing a first semiconductor layer over the workpiece;

forming a hard mask layer over the first semiconductor layer;

patterning the hard mask layer with a pattern for at least one bottom electrode in the at least one capacitor region and a pattern for at least one floating gate in the at least one transistor region;

forming a first poly-oxide region over the pattern for each at least one floating gate and forming a second poly-oxide region over the pattern for each at least one bottom electrode, the first poly-oxide region having a top surface and the second poly-oxide region having a top surface;

removing the hard mask layer, leaving portions of the first semiconductor layer exposed;

removing the exposed portions of the first semiconductor layer to form at least one floating gate in the at least one transistor region and at least one bottom electrode in the at least one capacitor region, the at least one floating gate comprising sidewalls and the at least one bottom electrode comprising sidewalls;

forming a first oxide layer over the top surface of the first poly-oxide region, the top surface of the second poly-oxide region, the sidewalls of the at least one bottom electrode, and the sidewalls of the at least one floating gate;

removing the first oxide layer and the second poly-oxide region in the at least one capacitor region;

forming a second oxide layer over at least the at least one capacitor bottom electrode in the capacitor region;

depositing a second semiconductor layer over the second oxide layer; and

removing portions of the second semiconductor layer to form a control gate proximate each at least one floating gate in the at least one transistor region and a top electrode over each bottom electrode in the at least one capacitor region.

2. The method according to Claim 1, wherein removing the first oxide layer and the second poly-oxide region in the at least one capacitor region comprises:

depositing a nitride layer over the first oxide layer;

removing a portion of the nitride layer to expose at least a portion of the at least one bottom electrode in the capacitor region;

removing the first oxide layer and the second poly-oxide region from over a top surface of the bottom electrode; and

removing at least portions of the nitride layer.

3. The method according to Claim 2, wherein removing the first oxide layer and the second poly-oxide region further comprises removing the first oxide layer from the sidewalls of the bottom electrode.

4. The method according to Claim 2, wherein removing the first oxide layer and the second poly-oxide region comprises a wet dip etch process.

5. The method according to Claim 2, wherein forming the hard mask layer and depositing the nitride layer comprise depositing silicon nitride.

6. The method according to Claim 2, wherein removing at least portions of the nitride layer comprises leaving a spacer comprising the nitride layer on the sidewalls of the at least one floating gate.

7. The method according to Claim 6, wherein removing at least portions of the nitride layer comprises an anisotropic etch process.

8. The method according to Claim 1, wherein depositing the first semiconductor layer and the second semiconductor layer comprise depositing polysilicon.

9. The method according to Claim 1, wherein forming the first oxide layer and the second oxide layer comprise forming silicon dioxide.

10. The method according to Claim 1, wherein patterning the hard mask layer comprises depositing a first photoresist layer over the hard mask layer, patterning the first photoresist layer, and using the first photoresist layer to pattern the hard mask layer, and wherein removing portions of the second semiconductor layer comprises depositing a second photoresist layer over the second semiconductor layer, patterning the second photoresist layer, and using the second photoresist layer to pattern the second semiconductor layer.

11. The method according to Claim 1, wherein removing the exposed portions of the first semiconductor layer comprises using the first poly-oxide region and the second poly-oxide region as a mask to pattern the first semiconductor layer.

12. The method according to Claim 1, wherein the workpiece includes at least one periphery circuit region, wherein removing the portions of the second semiconductor layer further comprises forming at least one gate of a transistor in the at least one periphery circuit region.

13. The method according to Claim 1, wherein forming the at least one floating gate in the at least one transistor region and forming the at least one bottom electrode in the at least one capacitor region comprise using a single lithography mask to pattern the first semiconductor layer.

14. The method according to Claim 1, wherein forming the control gate in the at least one transistor region and forming the top electrode over each bottom electrode in the at least one capacitor region comprise using a single lithography mask to pattern the second semiconductor layer.

15. The method according to Claim 1, wherein forming the first poly-oxide region and forming the second poly-oxide region comprise a wet oxidation process.

16. The method according to Claim 1, wherein the method includes forming a split gate transistor in the at least one transistor region, the split gate transistor comprising the floating gate, a gate oxide comprised of the first oxide layer, and the control gate, and wherein the method includes forming a polysilicon-insulator-polysilicon (PIP) capacitor in the at least one capacitor region, the PIP capacitor comprising the bottom electrode, a capacitor dielectric comprising the second oxide layer, and the top electrode.

17. The method according to Claim 16, wherein forming the split gate transistor comprises forming a flash memory device.

18. The method according to Claim 16, further comprising forming a third oxide layer over the workpiece, before depositing the first semiconductor layer, wherein the third oxide layer comprises a tunnel oxide in at least the transistor region.

19. The method according to Claim 18, wherein forming the third oxide layer comprises a thermal oxidation process.

20. A method of forming a polysilicon-insulator-polysilicon (PIP) capacitor, the method comprising:

providing a workpiece, the workpiece including at least one capacitor region and at least one transistor region;

forming a first oxide layer over the workpiece;

depositing a first polysilicon layer over the first oxide layer;

forming a mask layer over the first polysilicon layer, the mask layer comprising a pattern for at least one bottom electrode in the at least one capacitor region and a pattern for at least one floating gate in the at least one transistor region;

forming a first poly-oxide region over the pattern for each at least one floating gate and forming a second poly-oxide region over the pattern for each at least one bottom electrode, the first poly-oxide region having a top surface and the second poly-oxide region having a top surface;

removing the mask layer, leaving portions of the first polysilicon layer exposed;

using the first poly-oxide region and the second poly-oxide region as a mask to remove the exposed portions of the first polysilicon layer and form at least one floating gate in the at least one transistor region and at least one bottom electrode in the at least one capacitor region, the at least one floating gate comprising sidewalls and the at least one bottom electrode comprising sidewalls;

forming a second oxide layer over the top surface of the first poly-oxide region, the top surface of the second poly-oxide region, the sidewalls of the at least one bottom electrode, the sidewalls of the at least one floating gate, and the first oxide layer;

depositing a second nitride layer over the second oxide layer;

removing a portion of the second nitride layer to expose at least a portion of the second poly-oxide region over the bottom electrode in the capacitor region;

removing the second oxide layer and the second poly-oxide region from over a top surface of the bottom electrode in the at least one capacitor region;

removing at least portions of the second nitride layer, leaving a spacer comprising the second nitride layer on the sidewalls of the at least one floating gate;

forming a third oxide layer over at least the at least one capacitor bottom electrode in the capacitor region;

depositing a second polysilicon layer over the third oxide layer;

depositing a second photoresist layer over the second polysilicon layer;

patterning the second photoresist layer; and

using the second photoresist layer to pattern the second polysilicon layer, forming a control gate proximate each at least one floating gate in the at least one transistor region, and forming a top electrode over each bottom electrode in the at least one capacitor region, wherein the bottom electrode, the top electrode, and the third oxide layer disposed between the bottom electrode and top electrode comprise a PIP capacitor.

21. The method according to Claim 20, wherein removing the second oxide layer and the second poly-oxide region further comprises removing the second oxide from the sidewalls of the bottom electrode.

22. The method according to Claim 20, wherein removing the second oxide layer and the second poly-oxide region comprises a wet dip etch process.

23. The method according to Claim 20, wherein forming the first oxide layer, the second oxide layer and the third oxide layer comprise forming silicon dioxide.

24. The method according to Claim 23, wherein forming the first oxide layer comprises a thermal oxidation process.

25. The method according to Claim 20, wherein the workpiece includes at least one periphery circuit region, wherein patterning the second polysilicon layer further comprises forming at least one gate of a transistor in the at least one periphery circuit region.

26. The method according to Claim 20, wherein forming the first poly-oxide region and forming the second poly-oxide region comprise a wet oxidation process.

27. The method according to Claim 20, wherein the method includes forming a split gate transistor in the at least one transistor region, the split gate transistor comprising the floating gate, a gate oxide comprised of the second oxide layer, and the control gate.

28. The method according to Claim 27, wherein forming the split gate transistor comprises forming a flash memory device.

29. The method according to Claim 20, wherein the first oxide layer comprises a tunnel oxide in at least the transistor region.

30. A semiconductor device, comprising:

a workpiece, the workpiece including at least one capacitor region and at least one transistor region;

a first oxide layer formed over the workpiece;

a floating gate disposed over the first oxide layer in the at least one transistor region, the floating gate comprising sidewalls;

a bottom electrode disposed over the first oxide layer in the at least one capacitor region, the floating gate and bottom electrode being formed from a first semiconductor layer;

a poly-oxide region disposed over the floating gate, the poly-oxide region having a top surface;

a second oxide layer disposed over the top surface of the poly-oxide region and the sidewalls of the at least one floating gate in the at least one transistor region;

a third oxide layer disposed over the bottom electrode in the at least one capacitor region and over the first oxide layer in the at least one transistor region;

a control gate proximate the floating gate in the at least one transistor region; and

a top electrode disposed over each bottom electrode in the at least one capacitor region, the control gate and the top electrode being formed from a second semiconductor layer.

31. The semiconductor device according to Claim 30, further comprising a spacer disposed over the second oxide layer on the sidewalls of the floating gate.

32. The semiconductor device according to Claim 31, wherein the spacer comprises a nitride.

33. The semiconductor device according to Claim 30, wherein the first oxide layer, second oxide layer, and the third oxide layer comprise silicon dioxide.

34. The semiconductor device according to Claim 30, wherein the first semiconductor layer and the second semiconductor layer comprise polysilicon.

35. The semiconductor device according to Claim 30, wherein the workpiece includes at least one periphery circuit region, further comprising a transistor gate formed in the at least one periphery circuit region, the transistor gate being formed from the second semiconductor layer.

36. The semiconductor device according to Claim 30, wherein the device includes a split gate transistor in the at least one transistor region, the split gate transistor comprising the floating gate, a gate oxide comprised of the first oxide layer, and the control gate, and wherein the device includes a polysilicon-insulator-polysilicon (PIP) capacitor in the at least one capacitor region, the PIP capacitor comprising the bottom electrode, a capacitor dielectric comprising the third oxide layer, and the top electrode.

37. The semiconductor device according to Claim 36, wherein the split gate transistor comprises a flash memory device.